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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,121	01/15/2002	Brian Keith Owens	2001-0273.00	1297

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EXAMINER	
KANG, ROBERT N	

ART UNIT	PAPER NUMBER
2625	

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,121	OWENS ET AL.	
	Examiner	Art Unit	
	Robert N. Kang	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,12 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-18* is/are allowed.

6)☒ Claim(s) *6, 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Examiner has, upon further examination of the application, discovered issues which require a new office action and grounds for rejection. Examiner apologizes for the subsequent increase in prosecution due to this office action and as such this action is **non-final.**

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The final paragraph of both claims 6 and 12, "wherein the Flash to ROM interface passes through the status and read commands to the ROM memory cells but only indicates a ready status without passing through the write command to the ROM memory cells." The term "passes through" is indefinite; it is unclear what commands are passed "through." The commands, as depicted in FIG. 1, are sent from the printer-controller ASIC 32 to the Flash-to-ROM interface 18, which in turn decodes the opcodes and accesses the memory. Thus, the instructions are not "passed through."

Additionally, regarding the limitation, "the Flash to ROM interface... only indicates a ready status without passing through the write command to the ROM memory cells,"

is indefinite because it is unclear whether the word "only" indicates that the Flash to ROM interface suppresses a write command (i.e., the Flash to ROM interface cannot indicate status when a write command is issued), or whether the claim is merely stating that the status may be polled without requiring a coinciding write command. Examiner assumes the latter, since the suppression of a write command or mutual exclusivity of the write command and status indication is unsupported by the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Ali (US-PAT 6,016,472).

With regards to limitation 1, Ali discloses in figure 3 a DSP 310, with its own integral ROM 312, communicably attached through serial interface 122 to a flash memory unit 120 having internal non-volatile storage 324. Broadly defined, a "memory module" is a self-contained device capable of storing digital data. Therefore, the entire invention as disclosed by Ali qualifies as a type of memory module. The program ROM 312 meets the criteria of limitation (a), since the recited memory module comprises "a read only memory (ROM memory) cells." Furthermore, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the

flash memory unit 120, which qualifies as non-ROM. Therefore serial interface 122 is a "ROM to non-ROM interface," as required by limitation (b).

Regarding limitation 2, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120, which qualifies as an EPROM. Therefore serial interface 122 is a "ROM to EPROM interface." This is inconsistent with the generally accepted definition of an EPROM, which requires that the erase operation occur through the use of ultraviolet light. However, because the applicant's disclosed claim 3 identifies that Flash memory is an EPROM, the examiner is consistent with the applicant's strict interpretation of an EPROM as any memory which is erasable, programmable, and read-only.

Regarding limitation 3, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120. Therefore serial interface 122 is a "ROM to Flash interface."

Regarding limitation 4, because the program ROM 312 controls the DSP 310's operation and is encapsulated within the DSP block 110, the ROM 312 is operatively connected to the Flash memory unit 120 through serial interface 122. Therefore the "Flash to ROM interface is a serial interface."

In regards to limitation 5, Ali details the various connections of serial interface 122 in figure 2. In column 5, lines 31-32, Ali states "a chip select (CS) input is driven to a low logic state to indicated the beginning of a command to the flash memory." This input qualifies as "a Flash chip select transmission line," as claimed in line 3. Ali discloses in lines 37-51, "a serial clock (SCK) input on the flash memory unit 120 is

driven by a second bit input/output BIO1 on the DSP... A serial input (SI) line on the flash memory unit 120 is driven by a third bit input/output BIO2 on the DSP... A serial output (SO) line on the flash memory unit 120 drives a fourth bit input/output BIO3." These transmission lines are congruous to the "clock transmission line, flash serial input transmission line," and "flash serial output transmission line," as claimed in lines 2-3. Ali also discloses in column 5, lines 55-61, "a reset (RESET input on the flash memory unit 120 is coupled to the sixth bit input/out BIO6 on the DSP," which is identical to the function and operation of the applicant's disclosed "flash reset transmission line." Ali also describes "a ready/busy (RDY/BUSY) output from the flash memory unit 120 to a seventh bit input/output BIO6." This qualifies as "a status command." Finally, Ali depicts in figure 3 flash buffers 320 and 322, which serve to store input/output data. In column 10, lines 44-51, Ali states "data is passed from the DSP to the flash memory unit by setting the SI logic level appropriately before the SCK line is driven from low to high... data is passed from the flash memory unit 120 to the DSP 110 by setting the SO logic level appropriately before the SCK line is driven from low to high." These commands qualify as "read" and "write" commands for the Flash input transmission line.

Regarding limitation 6, the examiner assumes (see rejection under 35 U.S.C. § 112) the invention is merely capable of indicating the value of the status register without issuing a write command to the ROM memory cells. Ali discloses in column 8, lines 34-39, "before programming the flash buffer into the flash memory, the status of the flash memory unit is monitored to determine whether the prior programming operation (if any) has completed. The newly filled flash buffer cannot be programmed until the prior

programming option is finished." Thus Ali's invention meets the requirements of limitation 6. Additionally, several memory structures well known in the industry poll the status of a memory without issuing a write command (official notice), and thus the claimed feature is unpatentable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima (US-PAT 6,250,827) in view of Ali (US-PAT 6,016,472).

Regarding limitation 1, Nojima discloses in paragraph (249), "In FIG. 45, reference numeral 500 designates an ASIC in which the MPU part and printer control part are integrated. Numeral 504 represents a flash ROM which stores programs for controlling the whole of the recording device, numeral 505 a mask ROM storing character fonts etc., and numeral 506 a DRAM used as a work area of the ASIC 500 and as a buffer of signal. Numeral 509 denotes an EEPROM, this EEPROM 509 being a rewritable ROM which can retain the contents without supply of power." Therefore Nojima's invention qualifies as "a printer-controller ASIC having non-ROM memory control."

Nojima does not disclose a "memory module including ROM memory cells and a non-ROM to ROM interface operatively connected to the ROM memory cells, and a transmission cable operatively connected to the non-ROM memory control of the printer controller ASIC and the non-ROM to ROM interface of the memory module."

Ali discloses in figure 3 a DSP 310, with its own integral ROM 312, communicably attached through serial interface 122 to a flash memory unit 120 having internal non-volatile storage 324. Broadly defined, a "memory module" is a self-contained device capable of storing digital data. Therefore, the entire invention as disclosed by Ali qualifies as a type of memory module. The program ROM 312 meets the criteria of limitation (a), since the recited memory module comprises "a read only memory (ROM memory) cells." Furthermore, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120, which qualifies as non-ROM. Therefore serial interface 122 is a "ROM to non-ROM interface," as required by limitation (b).

Nojima and Ali are combinable because they both deal with ROM memory management in low cost devices such as printer ASICs and voice answering machines.

It would have been obvious at the time of invention to one of normal skill in the art to implement in Nojima's printing system Ali's memory module by replacing the DSP with the printer ASIC in the memory module block diagram.

The motivation of this modification would be to allow easy debugging and changes to the internal program memory of the print ASIC through the Flash Memory.

Therefore it would have been obvious to combine Nojima and Ali to achieve the invention of limitation 1. For the purposes of convenience, for further rejections the above combination of the Nojima print ASIC containing the Ali memory module shall be referred to herein as the "Nojima/Ali combination."

In regards to limitation 2, the Nojima/Ali combination contains serial interface 122, which connects the ROM 312 (via the printer ASIC), to the flash memory unit 120, which qualifies as an EPROM. Therefore serial interface 122 is a "ROM to EPROM interface." This is inconsistent with the generally accepted definition of an EPROM, which requires that the erase operation occur through the use of ultraviolet light. However, because the applicant's disclosed claim 3 identifies that Flash memory is an EPROM, the examiner is consistent with the applicant's strict interpretation of an EPROM as any memory which is erasable, programmable, and read-only.
Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120. Therefore serial interface 122 is a "ROM to Flash interface."

Regarding limitations 3 and 4, because in the Nojima/Ali combination, the program ROM 312 controls the ASIC's operation and is encapsulated within the ASIC block, the ROM 312 is operatively connected to the Flash memory unit 120 through serial interface 122. Therefore the "Flash to ROM interface is a serial interface."

In regards to limitation 5, Ali details the various connections of serial interface 122 in figure 2, utilized between the ROM and Flash Memory of the Nojima/Ali combination. In column 5, lines 31-32, Ali states "a chip select (CS) input is driven to a

low logic state to indicated the beginning of a command to the flash memory." This input qualifies as "a Flash chip select transmission line," as claimed in line 3. Ali discloses in lines 37-51, "a serial clock (SCK) input on the flash memory unit 120 is driven by a second bit input/output BIO1... A serial input (SI) line on the flash memory unit 120 is driven by a third bit input/output BIO2... A serial output (SO) line on the flash memory unit 120 drives a fourth bit input/output BIO3." These transmission lines are congruous to the "clock transmission line, flash serial input transmission line," and "flash serial output transmission line," as claimed in lines 2-3. Ali also discloses in column 5, lines 55-61, "a reset (RESET input on the flash memory unit 120 is coupled to the sixth bit input/out BIO6 on the DSP," which is identical to the function and operation of the applicant's disclosed "flash reset transmission line." Ali also describes "a ready/busy (RDY/BUSY) output from the flash memory unit 120 to a seventh bit input/output BIO6." This qualifies as "a status command." Finally, Ali depicts in figure 3 flash buffers 320 and 322, which serve to store input/output data. In column 10, lines 44-51, Ali states "data is passed from the DSP to the flash memory unit by setting the SI logic level appropriately before the SCK line is driven from low to high... data is passed from the flash memory unit 120 to the DSP 110 by setting the SO logic level appropriately before the SCK line is driven from low to high." These commands qualify as "read" and "write" commands for the Flash input transmission line, and are applicable in the Nojima/Ali combination wherein the printer ASIC replaces the DSP.

Regarding the final limitation, the examiner assumes (see rejection under 35 U.S.C. § 112) the invention is merely capable of indicating the value of the status

register without issuing a write command to the ROM memory cells. Ali discloses in column 8, lines 34-39, "before programming the flash buffer into the flash memory, the status of the flash memory unit is monitored to determine whether the prior programming operation (if any) has completed. The newly filled flash buffer cannot be programmed until the prior programming option is finished." Thus Ali's invention meets the requirements of limitation 6. Additionally, several memory structures well known in the industry poll the status of a memory without issuing a write command (official notice), and thus the claimed feature is unpatentable.

Allowable Subject Matter

4. Claims 14-18 are allowed.

5. The following is an examiner's statement of reasons for allowance: claim 14 under limitation b, line 5, states "the second memory module physically replaces the first memory module." Examiner can find no prior art of record wherein a finalized version of code is stored in a ROM and physically replaces the non-ROM memory which contained a non-final version of the development code, particularly in the context of a printer ASIC.

Several well-known examples of upgrading firmware utilize physically replacing a ROM or PROM with an identical unit having newer software contained thereon. However, replacing an EPROM with a ROM is typically unfounded in the art.

Additionally, the non-ROM to ROM interface disclosed in memory module 10 can be found in numerous applications, such as the HP 39594F#4350 compact-flash card, which includes a PDL or firmware on a ROM. A compact-flash card is well known as a

writable memory, and thus the interface between the card and the ROM of the memory module is well known. However, none of the relevant prior art of record indicates that this ROM physically replaces an EPROM containing the non-final version of program firmware.

Finally, classes 714/6, 365/185.29, and 365/185.33 contain numerous patents on implementing memory redundancy, wherein a physical block (meaning a contiguous region of a memory i.e., a section of circuits or switches) of memory replaces another physical block of memory due to failure or defect. However, these inventions generally pertain to a redundancy circuit wherein a logical replacement for physical blocks of memory is carried out; numerous references in this class specifically make the distinction between physical and logical replacement of memory.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

For the reasons stated in item 1, this action is NON-FINAL.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert N. Kang whose telephone number is 571-272-0593. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler M. Lamb can be reached on (571)272-7406. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RNK

Twyler M. Lamb
Supervisory Patent Examiner